AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages connected in series, each predetermined delay stage adds a predetermined delay time to ~~an input~~ a signal received by the predetermined delay stage; and

[[a]] two or more selecting switch sections, wherein an input terminal thereof is connected to an output terminal of each predetermined delay stage, each ~~at least one of the~~ selecting switch section ~~sections~~ comprises:

~~a buffer section for receiving delayed input signal from one of the delay stages; and~~

~~a selecting section means directly connected to the buffer section for activating the buffer section to establish a delay path, wherein~~

a selecting section means for selecting one of output terminals of the predetermined delay stages by control signal to receive a delayed input signal from the output terminal; and

a buffer section provided with first and second transistors, wherein

the delayed input signal is propagated to each gate of the first and second transistors via the selecting section means, and wherein

an output signal from ~~the delay path~~ the buffer section has a desired delay time.

Claims 2- 9 (Canceled)

10. (Currently Amended) The delay circuit according to Claim [[4]] 35, wherein the first power supply voltage is a power supply voltage potential and the first ~~and second transistors are~~ transistor is a PMOS ~~transistors~~ transistor.

11. (Currently Amended) The delay in circuit according to claim [[4]] 35, wherein the ~~first~~ second power supply voltage is a ground potential and the ~~first and~~ second transistor ~~transistors are~~ is an NMOS transistor ~~transistors~~.

Claims 12-17 (Canceled)

18. (Currently Amended) The delay circuit according to claim ~~16~~ 1, wherein ~~in at least one of the predetermined delay stages,~~ the rise ~~delay time~~ and the fall delay time ~~for a signal inputted to each of the predetermined delay stages~~ of the predetermined delay time are substantially uniform.

Claims 19-20 (Canceled)

21. (Currently Amended) The delay circuit according to claim ~~16~~ 32, wherein each of the predetermined delay stages comprises an even number of logic inversion sections connected in series, ~~in which~~ each logic inversion section having different propagation delay time between the rise ~~delay time~~ and fall transition ~~delay time of the signal are different.~~

22. (Currently Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NAND gate, each NAND gate having the same structure ~~that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a power supply voltage potential~~, and wherein a predetermined input terminal is connected to an output terminal of preceding NAND gate.

23. (Currently Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NOR gate, each NOR gate having the same structure ~~that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a ground potential~~ and wherein a predetermined input terminal is connected to an output terminal of preceding NOR gate.

Claims 24-25 (Canceled)

26. (Currently Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages connected in

series, each predetermined delay stage adds a predetermined delay time to ~~an input~~ a signal received by the predetermined delay stage; and

two or more selecting switch sections, wherein an input terminal thereof is connected to an output terminal of each predetermined delay stage, each

~~at least one of the~~ selecting switch sections comprises:

~~a buffer section for receiving delayed input signal from one of the delay stages; and~~

~~a selecting section means directly connected to the buffer section for activating the buffer section to establish a delay path, wherein~~

a selecting section means for selecting one of output terminals of the predetermined delay stages by control signal to receive a delayed input signal from the output terminal; and

a buffer section provided with first and second transistors, the delayed input signal is propagated to each gate of the first and second transistors via the selecting section means, wherein

an output signal from ~~the delay path~~ the buffer section has a desired delay time.

Claims 27- 31 (Canceled)

32. (Currently Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages connected in series, each of which is provided with an individual delay input terminal for inputting a signal to which predetermined delay time is added, ~~the signal inputted to~~ each

predetermined delay stage having substantially uniform rise delay time and fall delay time, and

selecting switch means connected to one of the individual delay input terminals and receiving an input signal ~~to the delay section~~ for establishing a delay path for the input signal by selecting one of the predetermined delay stages,

wherein an output signal from the delay path has a desired delay time.

Claims 33-34 (Canceled)

35. (New) The delay circuit according to claim 1, wherein the first transistor is connected between an output terminal outputting the output signal and a first power supply voltage, and the second transistor is connected between the output terminal and a second power supply voltage.

36. (New) The delay circuit according to claim 1, wherein each gate of the first and second transistors is controlled by a logical gate circuit.

37. (New) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages connected in series, each of which is provided with an individual delay input terminal for inputting a signal to which predetermined delay time is added, each predetermined delay stage having substantially uniform rise delay time and fall delay time; and

selecting switch means connected to one of the individual delay input terminals and receiving an input signal for establishing a delay path for the input signal by selecting one of the predetermined delay stages,

wherein an output signal from the delay path has a desired delay time.